REMARKS

The specification has been amended to more clearly state that vias 421 and 422 extend "below the surface 119 and" into layers 118, 117, 116, 115, and 112 (FIG.1). No new matter has been introduced.

Claims 1, 2, 4, 6-10, 12, 14, 16-21 remain in this application. Claims 3, 5, 11, 13, and 15 have been canceled. Claims 22-25 are withdrawn.

The undersigned has recently been assigned for handling of the above-identified patent application. Upon a thorough review of the docket file and the previous actions, the amendments presented herein above have been made and are believed to place the application in condition for allowance.

In particular, the prior art of record does not specifically teach or suggest all the claim elements of a method of manufacturing a semiconductor component comprising: "providing a delta-doped heteroepitaxial semiconductor structure substrate with a surface; providing a layer of undoped gallium arsenide on the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the layer having a thickness on the order of six to twelve nanometers; forming a gate contact on a first portion of the undoped gallium arsenide layer; and removing a second portion of the undoped gallium arsenide layer to expose a portion of the surface of the delta-doped heteroepitaxial semiconductor structure substrate, wherein the remaining first portion of the undoped gallium arsenide layer does not substantially extend beyond the horizontal profile of the gate contact".

Neither does the cited prior art specifically teach or suggest: "further forming a dielectric layer over the gate contact, the remaining first portion of the undoped gallium arsenide layer and the exposed portion of the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the dielectric layer having a thickness on the order of twenty to sixty nanometers; implanting source and drain regions through the dielectric layer and into the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the implant regions extending from the surface of the delta-doped heteroepitaxial semiconductor structure substrate into a buffer layer of the substrate but not extending into a support layer of the substrate, wherein the first portion of the undoped gallium arsenide layer remains undoped; annealing the source and drain regions, wherein annealing activates dopants in the implanted source and drain regions and increases a

density of the dielectric layer; and forming source and drain contacts over the source and drain regions in respective source and drain contact vias, the source and drain contact vias extending through the dielectric layer and extending from the surface of the delta-doped heteroepitaxial semiconductor structure substrate into the buffer layer of the substrate but not extending into the support layer of the substrate."

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

The Applicants believe that the subject application, as amended, is in condition for allowance. Such action is earnestly solicited by the Applicants.

In the event that the Examiner deems the present application non-allowable, it is requested that the Examiner telephone the Applicant's attorney, Michael J. Balconi-Lamica, at the number indicated below so that the prosecution of the present case may be advanced by the clarification of any continuing rejection.

Accordingly, this application is believed to be in proper form for allowance and an early notice of allowance is respectfully requested.

Please charge any fees due to **Deposit Account Number 502117.** The Deposit Account Name is **Motorola, Inc.**.

Respectfully submitted,

By: Michael J. Balconi-Lamica

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